REMARKS

Applicant respectfully requests reconsideration. Claims 1, 6 and 16-25 have been amended.

Objections to the Drawings

The Examiner objected to figures 1-3 for not being labeled as Prior Art. The Examiner has also objected to figures 3 and 4 for not having reference characters mentioned in the description. The label "Prior Art" has been added to figures 1-3. Reference "O5" has been added to figures 3 and 4. These changes correct obvious errors and do not add new matter. Accordingly, withdrawal of this objection is respectfully requested.

Claim Objections

The Examiner objected to claims 1 and 23 as containing informalities. These claims have been amended to correct the informalities. The changes are not intended to alter the scope of the claims. Accordingly, withdrawal of this objection is respectfully requested.

Rejections under 35 U.S.C. §112

The Examiner rejected claims 1 and 21 under 35 U.S.C. §112. Claim 1 is rejected for not providing sufficient antecedent basis for the limitations "the signals" and "the other means." The claim has been amended to correct this error, but the change is not intended to alter the scope of the claim.

Claim 21 is rejected because it duplicates claim 20. Claim 21 has been amended so as not to duplicate claim 20. Accordingly, withdrawal of the rejection of claims 1 and 21 under 35 U.S.C. §112 is respectfully requested.

Rejections Under 35 U.S.C. §102

The Examiner rejected claims 1-5 under 35 U.S.C. §102 as being anticipated by the background information stated in the present application (the "Background"). The Examiner has also rejected claims 16 and 24 under 35 U.S.C. §102 as being anticipated by Ahanin et al U.S. Patent No. 5,166,604.

Applicants disagree that the prior art shows all of the claimed features. FIG. 3 of the present application shows a prior art circuit with disturbing elements such as 2, 5 and 8 all disabled by one signal, identified as "TEST." The reference does not describe separate inhibition of disturbing elements or a controller that can generate control signals for that purpose.

The Ahanin reference only shows control signals applied from off-chip. In the embodiment of FIG. 2, disabling signals are provided through terminals 12f, 12i and 12k. In the embodiment of FIG. 3, the reference shows disabling signals provided through input terminals of the device 12s...12z. In the embodiment of FIG. 4, the reference shows the disabling signals provided through the input terminals to the device 12f, 12i and 12k. These signals are not generated by a controller on the chip. The reference does not describe how those signals are generated or a specific control algorithm for generating those signals during a scan test.

Accordingly, the references do not show limitations in each of the independent claims. For example, claim 1 recites a "control means." The control means has a first operating mode and a second operating mode. The claim requires that in the first mode the control means operate "the test means in synchronism with a command signal while operating continuously the inhibition means." The claim further requires that in the second operating mode inhibition means of a first type operates "in synchronism with a command signal while operating continuously inhibition means of a type different from the first type and the test means, or for operating simultaneously the test means and inhibition means of a first type of the plurality of types of inhibition means in synchronism with the command signal while operating continuously inhibition means in synchronism with the command signal while operating continuously inhibition means of a type different from the first type."

The prior art of record does not describe or suggest a control means. The references therefore cannot provide any teaching of a control means with two operating modes. Nor can the references teach or suggest the specifics of the two modes recited in the claims. Accordingly, claim 1 cannot be said to be anticipated or obvious in light of the references.

Claims 2-5 depend from claim 1 and likewise should be allowed.

Claim 16 recites a scan test method. The claim recites that each of the "elements capable of disturbing a scan test" has a type. According to the method of the claim, disturbing elements are inhibited "except a plurality of disturbing elements of a selected type." The scan test is performed on "the disturbing elements of the selected type." The process of inhibiting and performing a scan test is repeated. The claim further requires that a scan test of the logic blocks be performed "with all of the disturbing elements inhibited."

The claimed method of controlling the disturbing elements while performing a scan test is not shown or suggested in the references. The background section of the present application shows structures in which the inhibiting elements are not separately controlled. The Ahanin reference describes no specific pattern of control of inhibiting elements during a scan test. Accordingly, it does not show or suggest the specifics of the claim. Accordingly, claim 16 should be allowed.

The references also do not show claimed features of claim 24. The claim depends from claim 16 and should be allowed for the reasons stated above. The claim adds further details of the manner in which the disturbing elements are controlled which are also not shown in the references.

Rejections Under 35 U.S.C. §103

The Examiner rejected claims 6, 7, 11-15, 19-23 and 26 under 35 U.S.C. §103(a) as being unpatentable over the Background in view of Ahanin et al U.S. Patent No. 5,166,604.

Claim 6 recites "a controller for successively controlling each of the inhibiting circuits individually during a scan test." As discussed above, neither reference shows a controller. Nor do the references deal with a specific method of controlling the scan test. Consequently, the references provide no teaching or suggestion of a controller meeting the other limitations of the claim. Even if the references are combined, the combination would not contain all limitations of the claim and claim 6 is not obvious in light of the references.

Claims 7 and 11-15 depend from claim 6. The dependent claims add limitations further distinguishing over the prior art. These claims should also be allowed.

Similarly, claims 19-23 depend from claim 16. As stated above, neither reference shows or suggests the features of claim 16. Claims 19-23 should be allowed for the same reasons given in connection with claim 16. The dependent claims add further limitations specifically relating to the types of disturbing elements that are not inhibited. Because the references do not teach the aspects of the independent claim relating to control of selected types of inhibiting elements, they do not provide teaching for these more specific recitations and should also be allowed.

The Examiner rejected claims 8-10, 17-18, and 25-26 under 35 U.S.C. 103(a) over the Background in view of Ahanin et al., U.S. Patent No. 5,166,604 and Nadeau-Dostie et al U.S. Patent No. 6,510,534.

Applicants disagree that the Nadeau-Dostie reference teaches the missing elements or is properly combinable with the other references. The Nadeau-Dostie reference relates to a method and apparatus for testing high performance circuits. The reference describes ways to generate a capture clock signal for test circuitry when the capture clock is not provided by a test system attached to the chip being tested. It does not relate to inhibiting disturbing elements in a logic block during a scan test. Though the reference could be from an analogous field, there is no motivation to combine the references.

Even if combined, the combination would not contain all the limitations of the claims. The reference describes that the capture clock generated for the test is provided to all of the scanned elements. It does not successively control each of the inhibiting circuits individually during a scan test in the manner recited in the claim.

The reference does not teach any of the claim elements that are not shown in the other references. For example, the reference does not teach "a controller for successively controlling each of the inhibiting circuits individually during a scan test" as recited in claim 6. Because claims 8-10 depend from claim 6 they incorporate this limitation and are not obvious. The dependent claims add further features for distinguishing over the prior art. For example, claims 8-10 recite additional limitations on the controller. Because the controller is not shown or suggested in the prior art these additional limitations are not shown or suggested by the reference either.

As to claims 17-18 and 25-26, these claims depend from claim 16. The Nadeau-Dostie reference does not teach the elements of claim 16 that are not found in the other references. For example, it provides no teaching in types of disturbing elements and a method of repeatedly

selecting a type of disturbing element and disabling disturbing elements except the selected type. Because the reference relates to generation of clock signals, it provides no teaching on this claim limitation.

The dependent claims add limitations further distinguishing over the prior art. The claims describe in greater detail performing a scan test on selected disturbing elements. Because selecting disturbing elements is not described in the references at all, there is no teaching of these additional limitations.

Accordingly, withdrawal of this rejection is respectfully requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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Date: December 16, 2004
x12/16/04x

In the Drawings

"Replacement Sheets" are attached which include a clean version of amended Figures 1, 2, 3 and 4. The attached sheets replace the original sheets including Figures 1, 2, 3 and 4.

"Annotated Sheets Showing Changes" are also attached which includes a marked-up version of Figures 1, 2, 3 and 4.

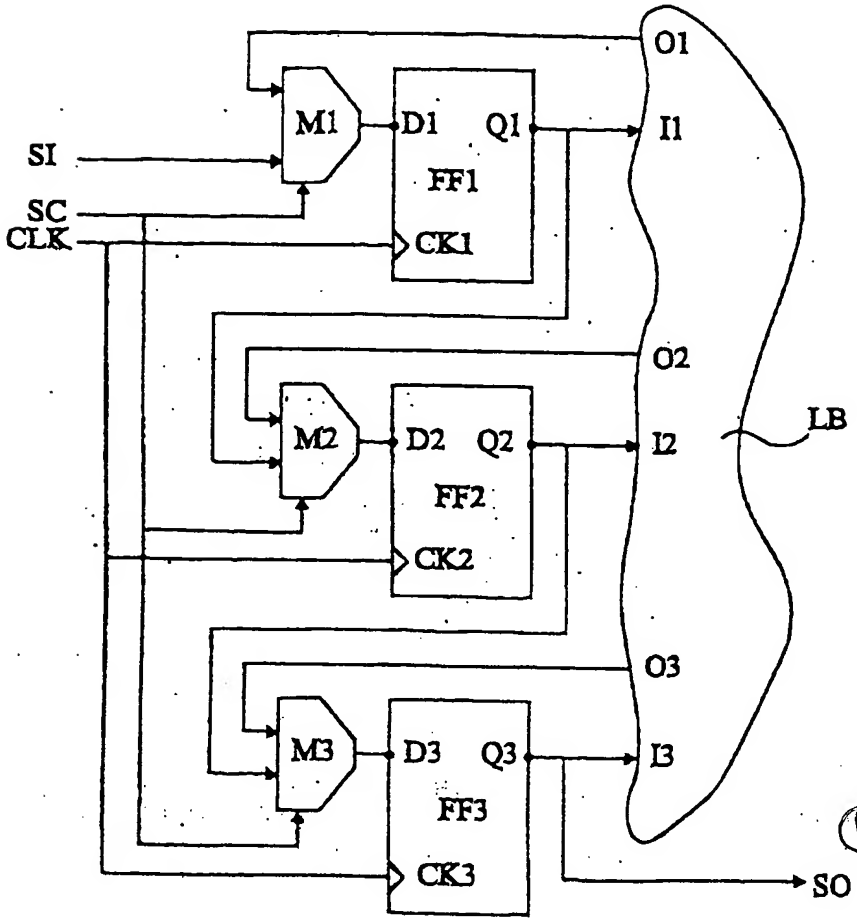

Fig 1
(prior art)

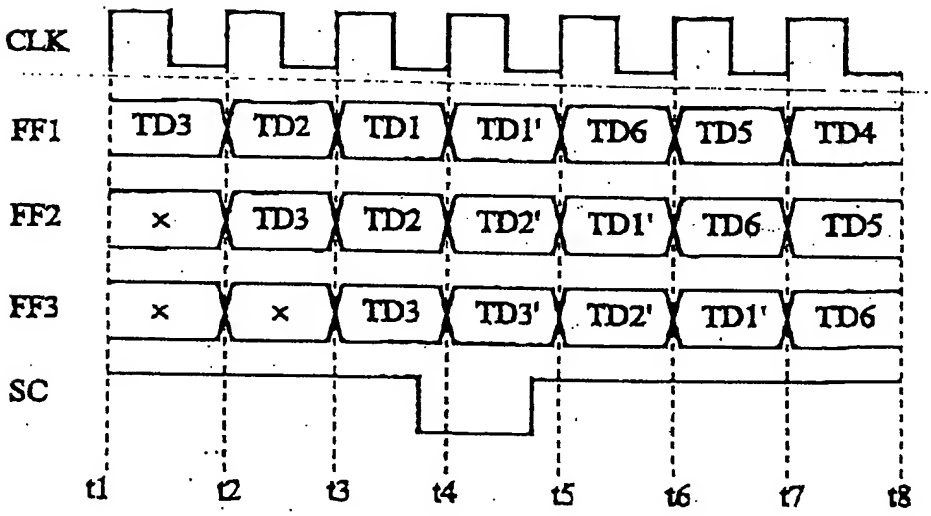

Fig 2
(prior art)

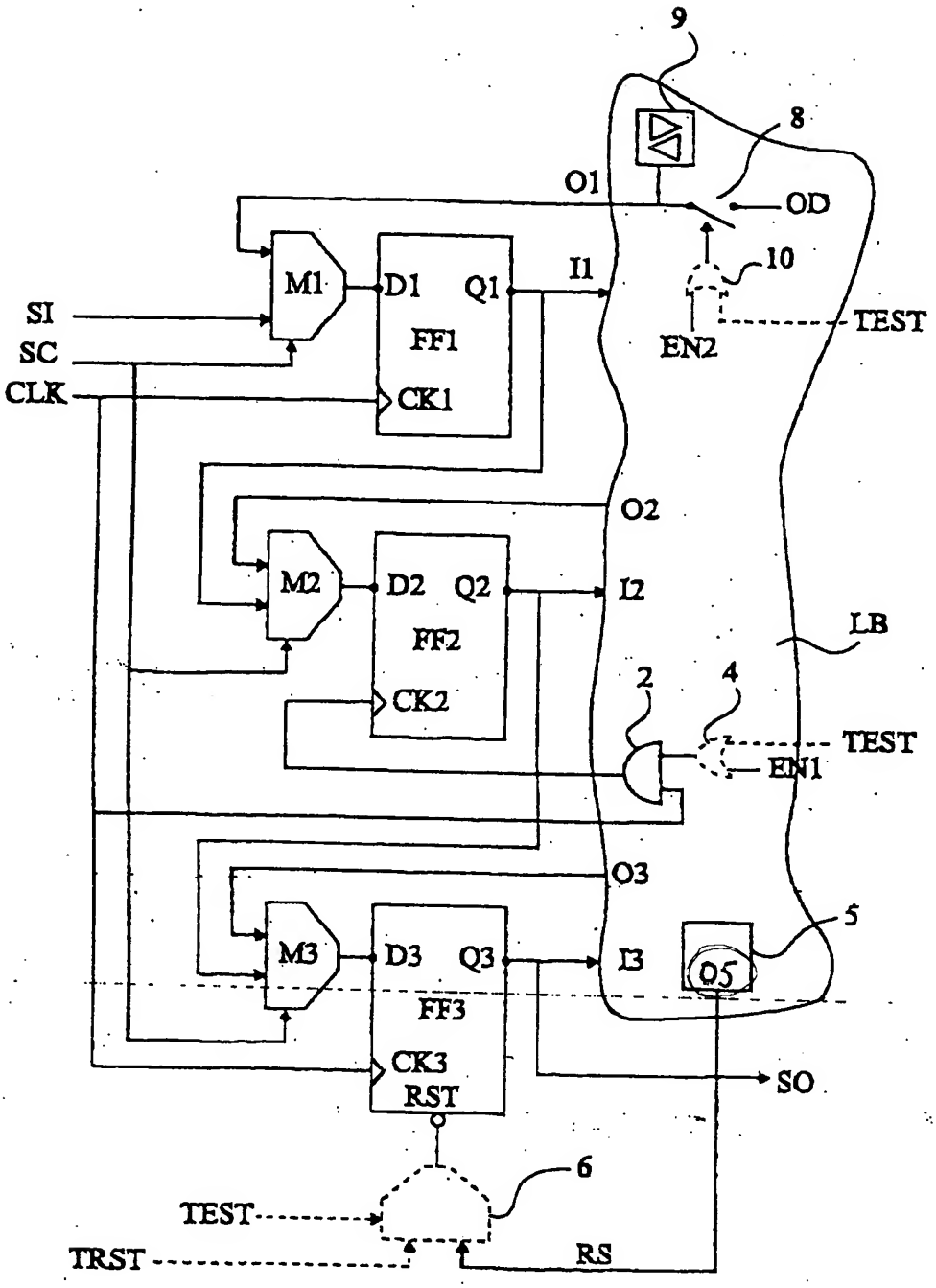

Fig 3
(prior art)

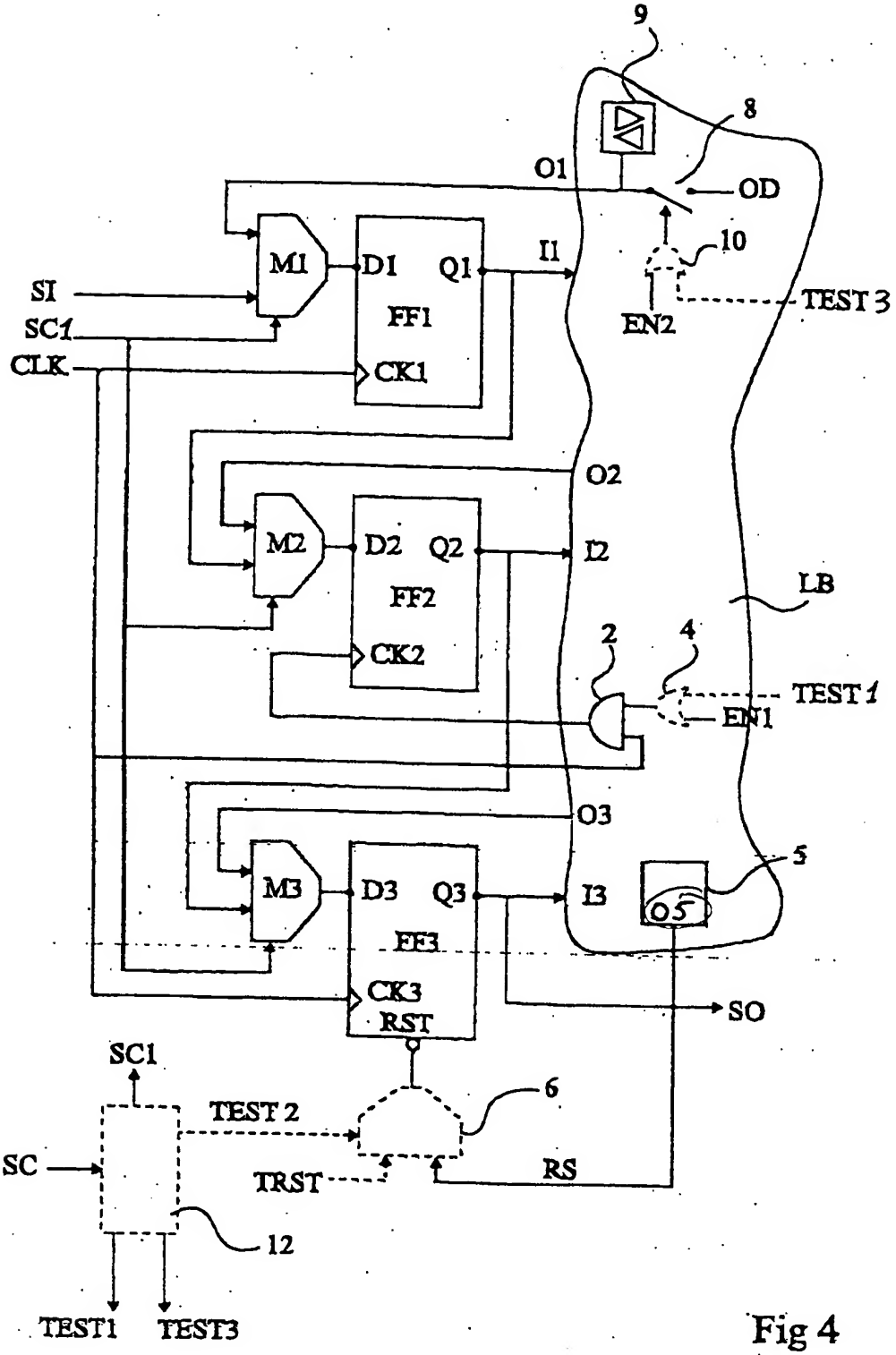
9
8
O1
OD
10
TEST 3
EN2
M1
D1
Q1
I1
SI
SC1
CLK
FF1
CK1
O2
M2
D2
Q2
I2
LB
2
4
TEST 1
EN1
FF2
CK2
O3
M3
D3
Q3
I3
5
05
FF3
CK3
RST
SO
SC1
TEST 2
6
SC
TRST
RS
12
TEST1
TEST3

Fig 4